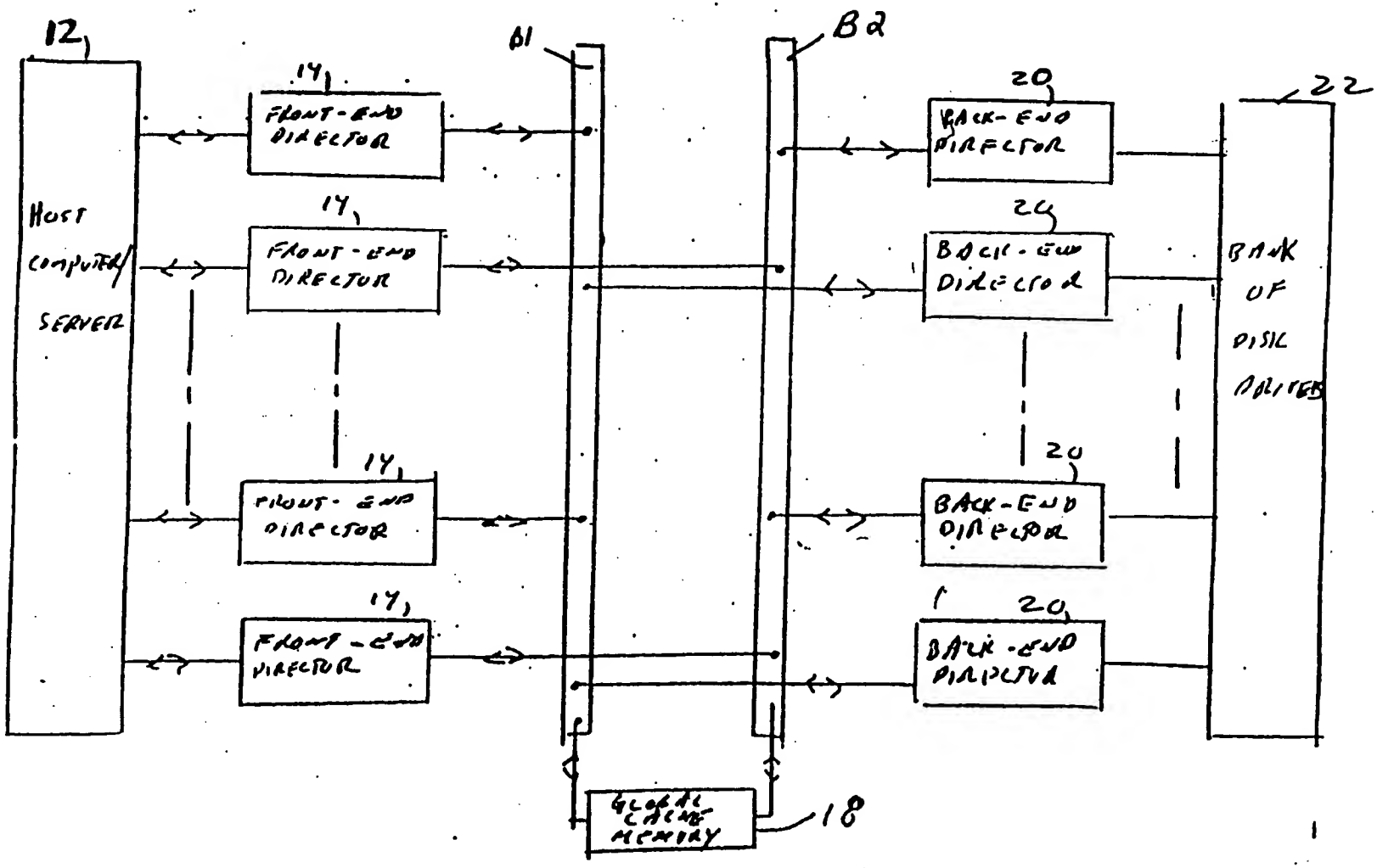
SCANNED, # 12

Christopher S. MacLellan et al.
METHOD FOR VALIDATING WRITE DATA
TO A MEMORY
Application No. 09/746,496

FIG. 1
PRIOR ART



SCANNED, # 12

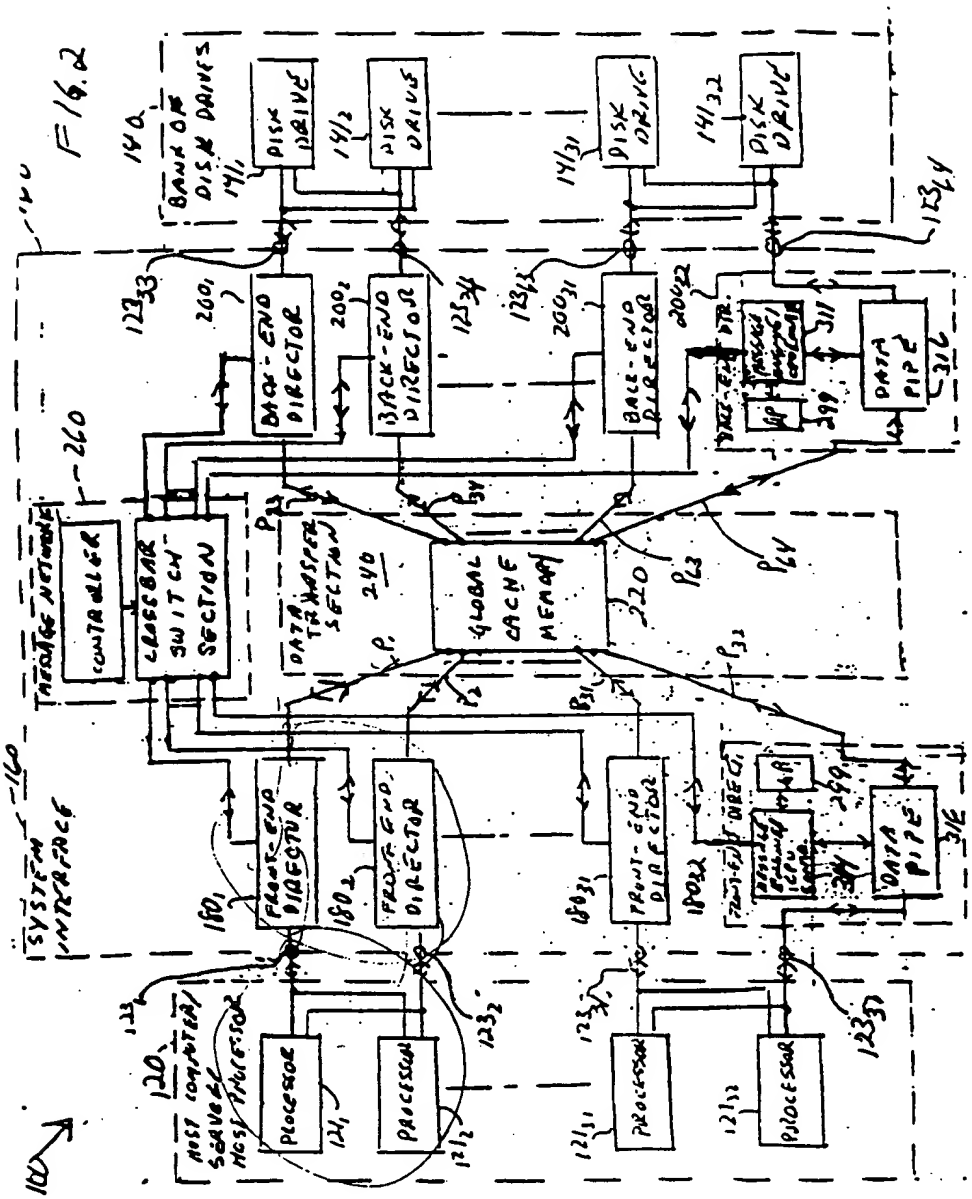


FIG. 2
DISK DRIVES
DISK DRIVE
BACK-END DIRECTOR
FRONT-END DIRECTOR
CROSSBAR SWITCH SECTION
GLOBAL CACHE MEMORY
DATA PIPE
PROCESSOR
HOST COMPUTER/ SERVER/ WEB PROTECTOR
SYSTEM INTERFACE
TARGET NETWORK

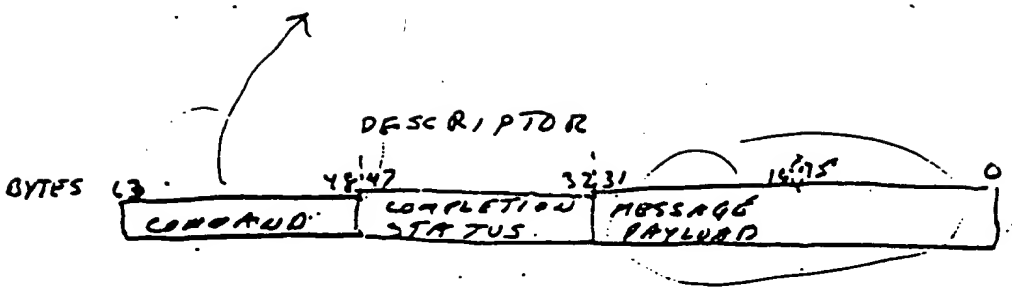

DESCRIPTOR
BYTES
63
48
47
32
31
16
15
0
COMMAND
COMPLETION STATUS
MESSAGE PAYLOAD

FIG 2A

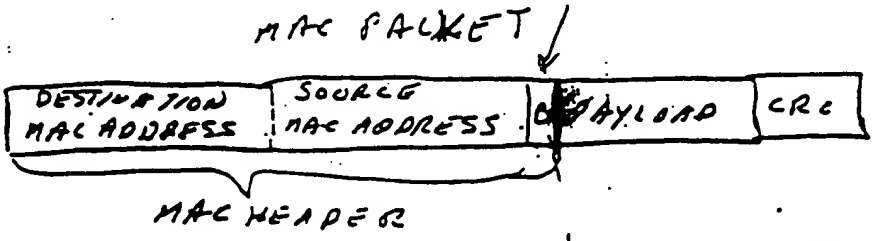

MAC PACKET
DESTINATION MAC ADDRESS
SOURCE MAC ADDRESS
PAYLOAD
CRC
MAC HEADER

FIG 2B

FIG. 3

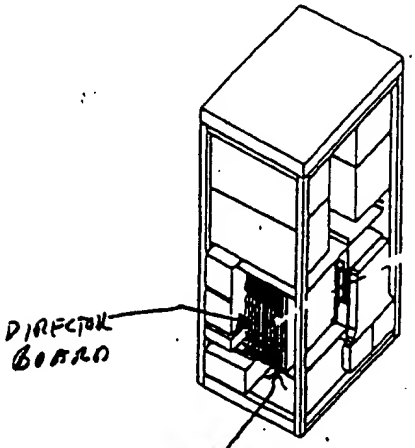
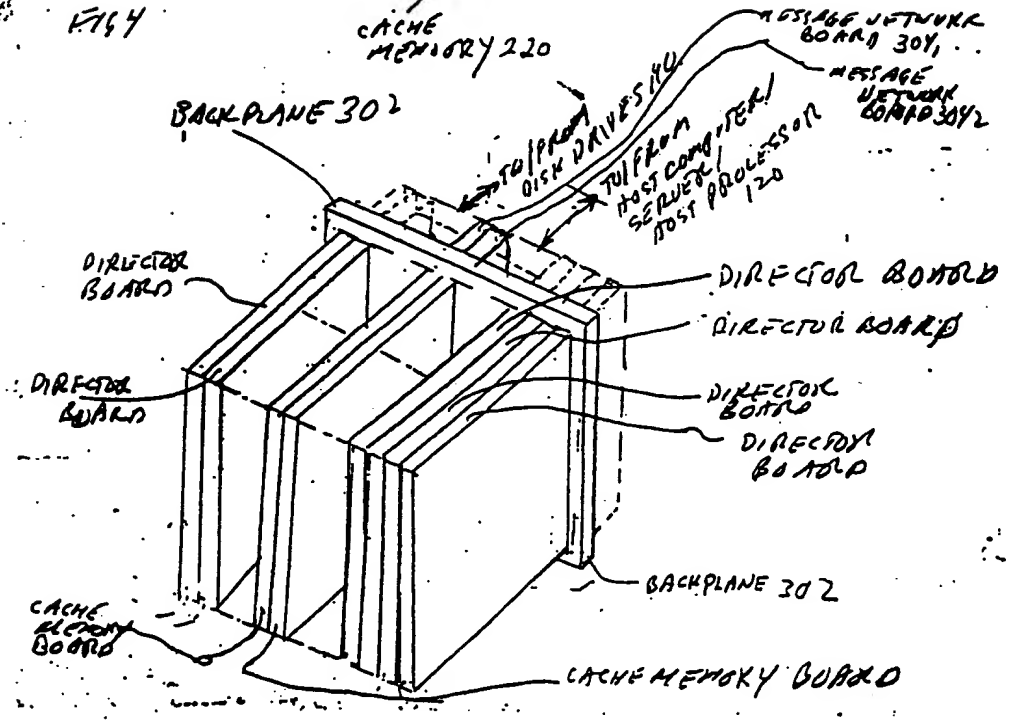
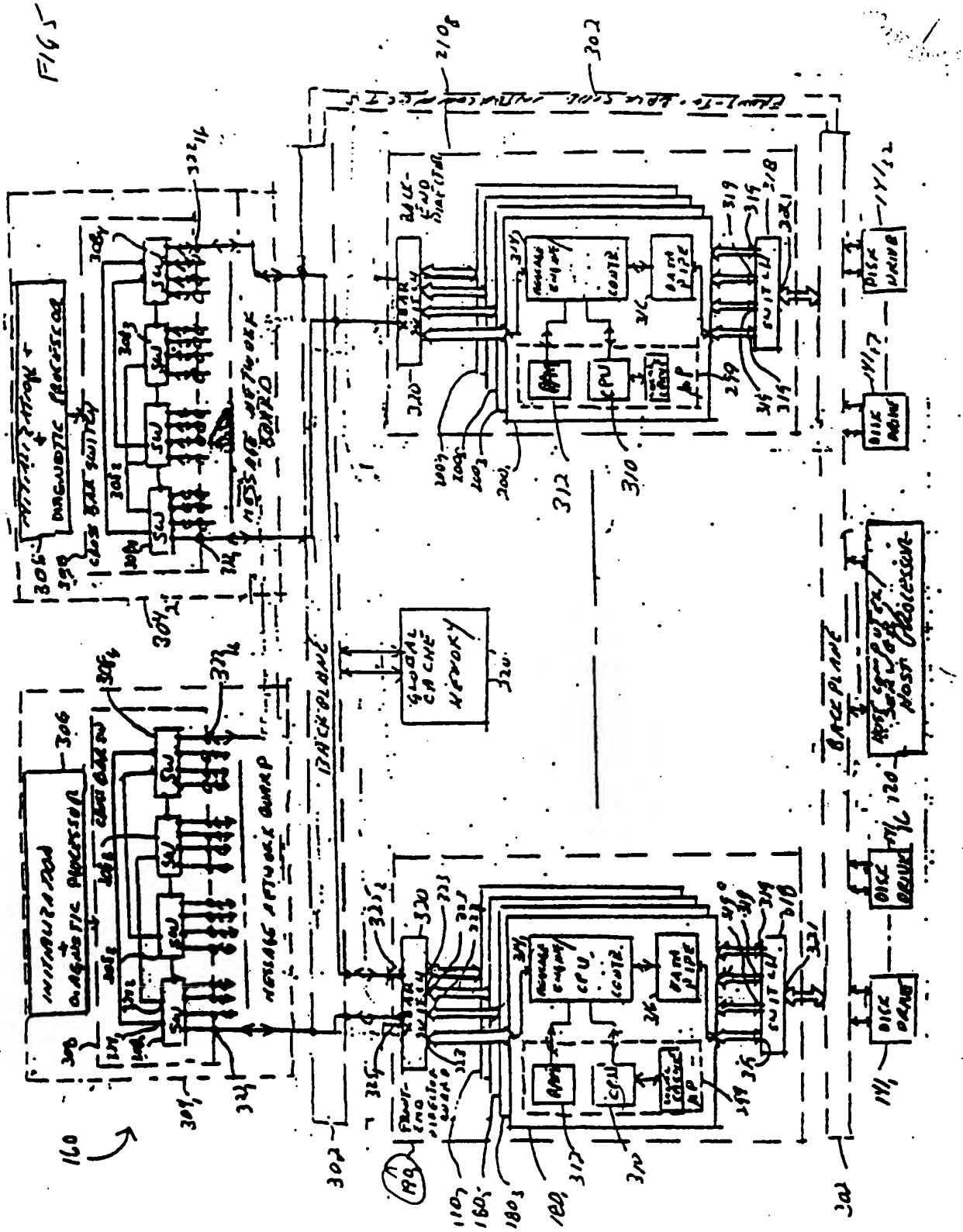
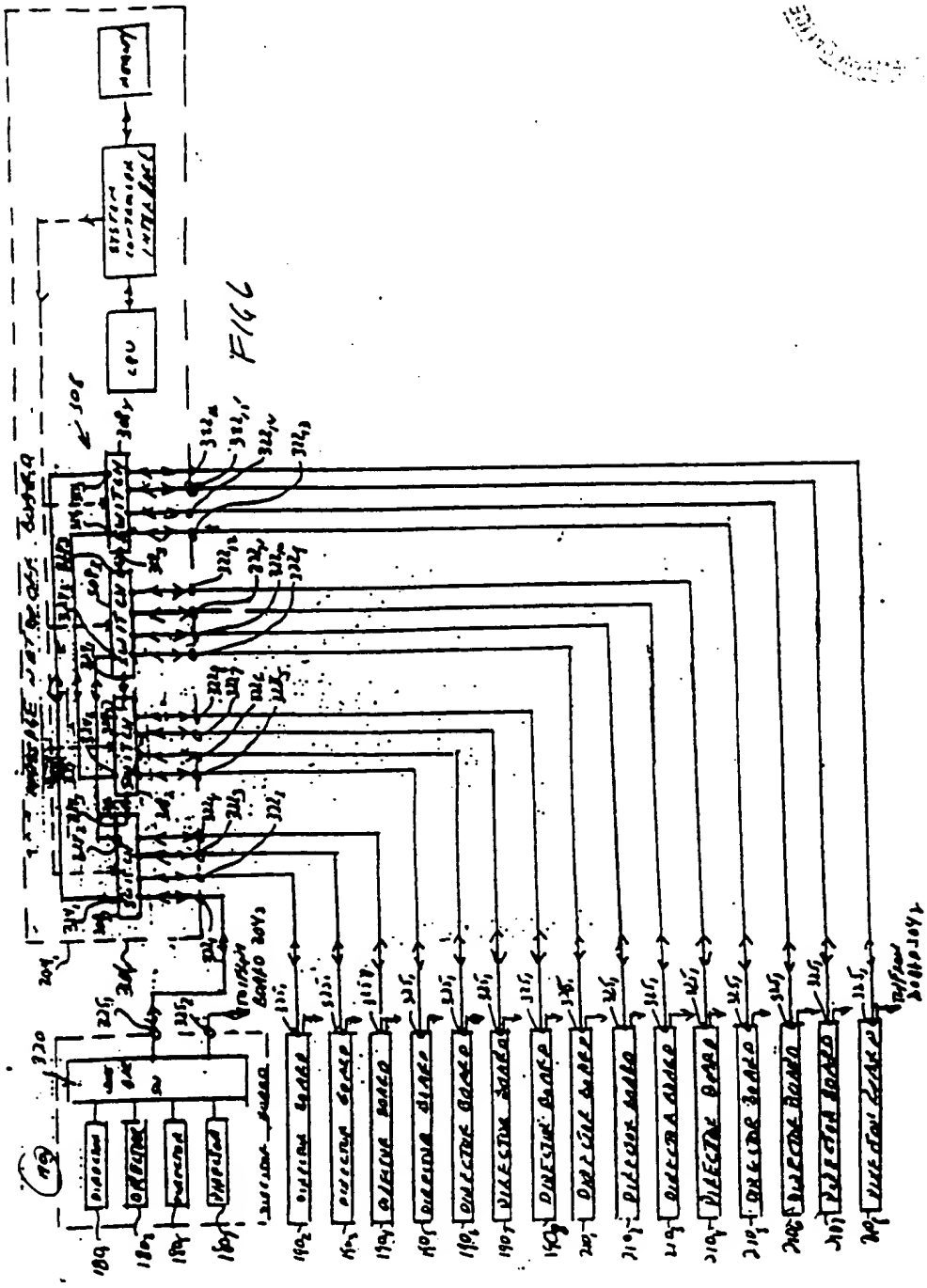

DIRECTOR BOARD

FIG 4


CACHE MEMORY 220
BACKPLANE 302
MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304,
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ HOST PROCESSOR 120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD





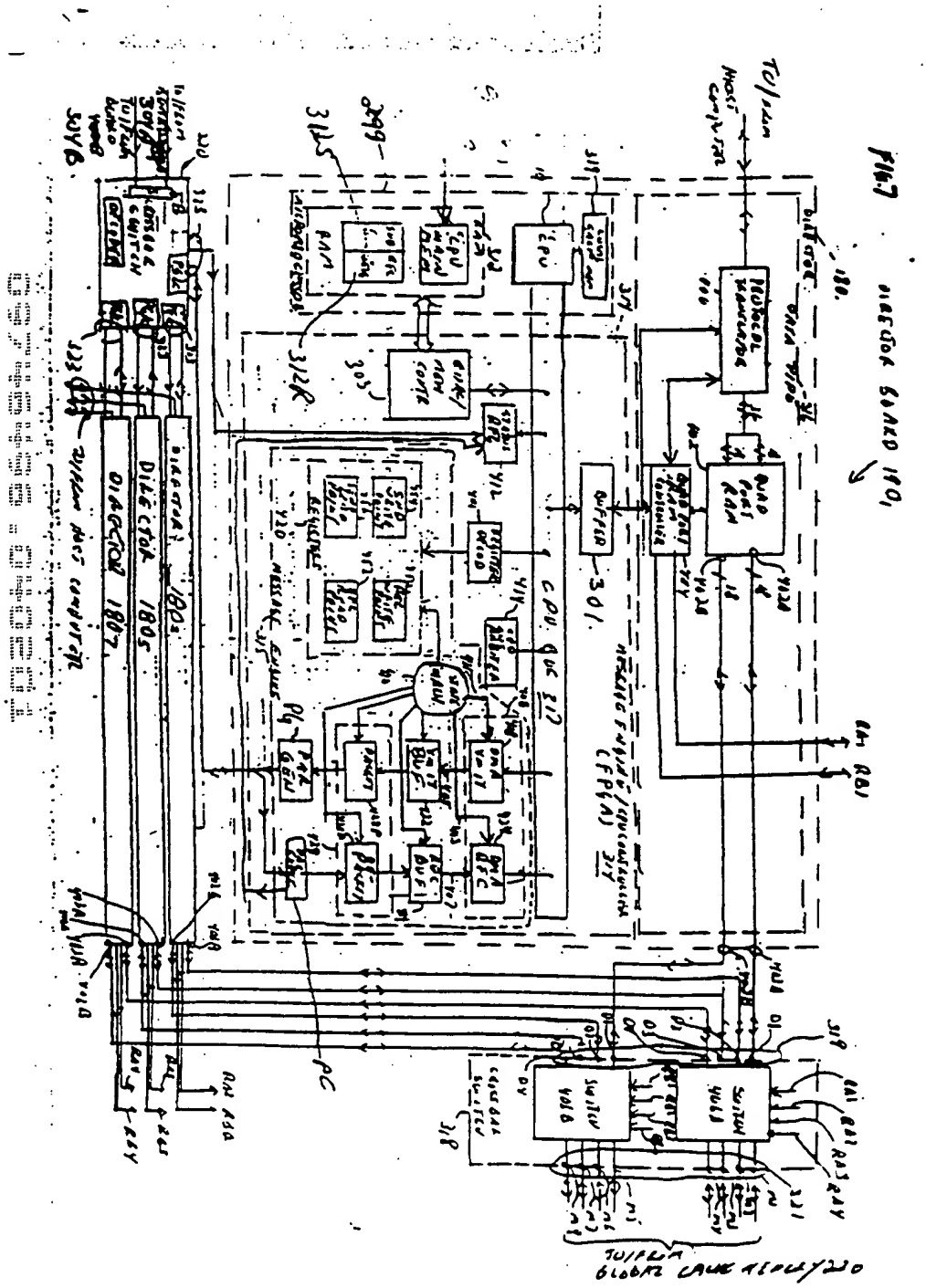
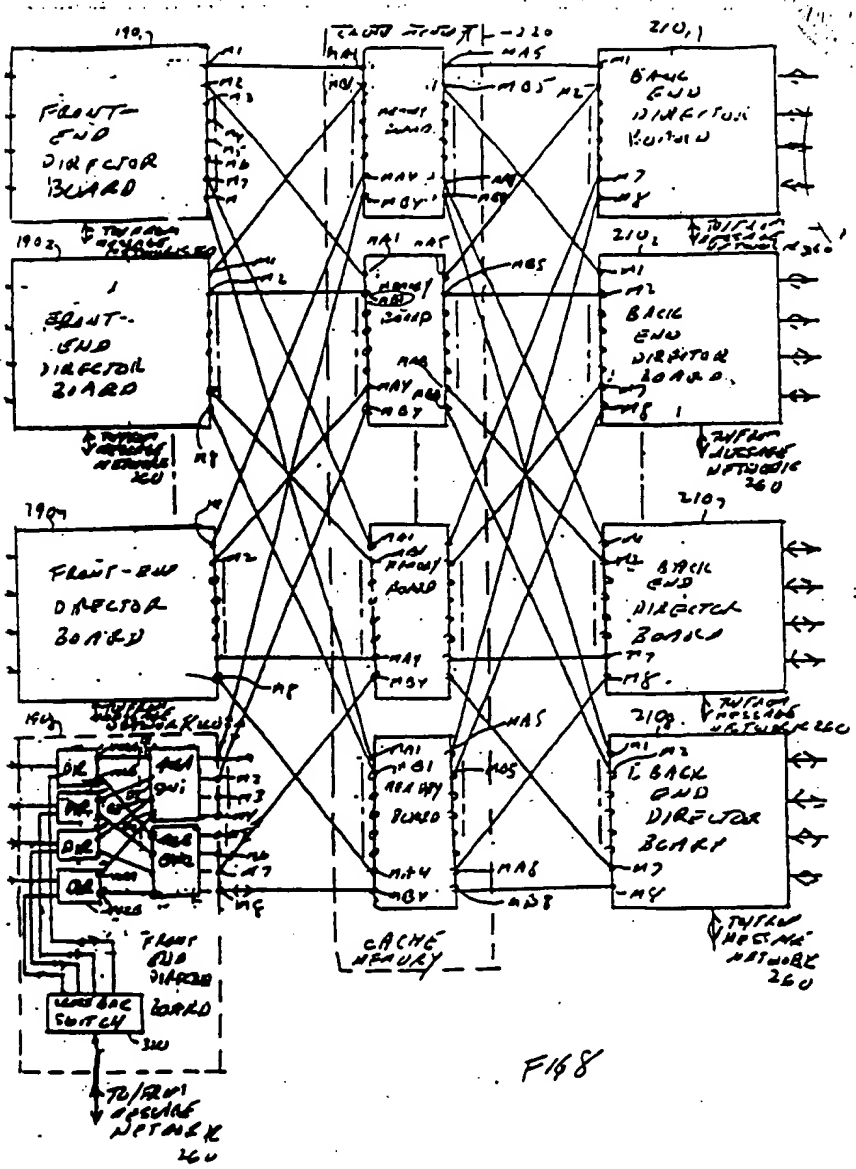


FIG. 7


FRONT-END DIRECTOR BOARD
BACK END DIRECTOR BOARD
CACHE MEMORY
FRONT END DIRECTOR BOARD
SWITCH

F168

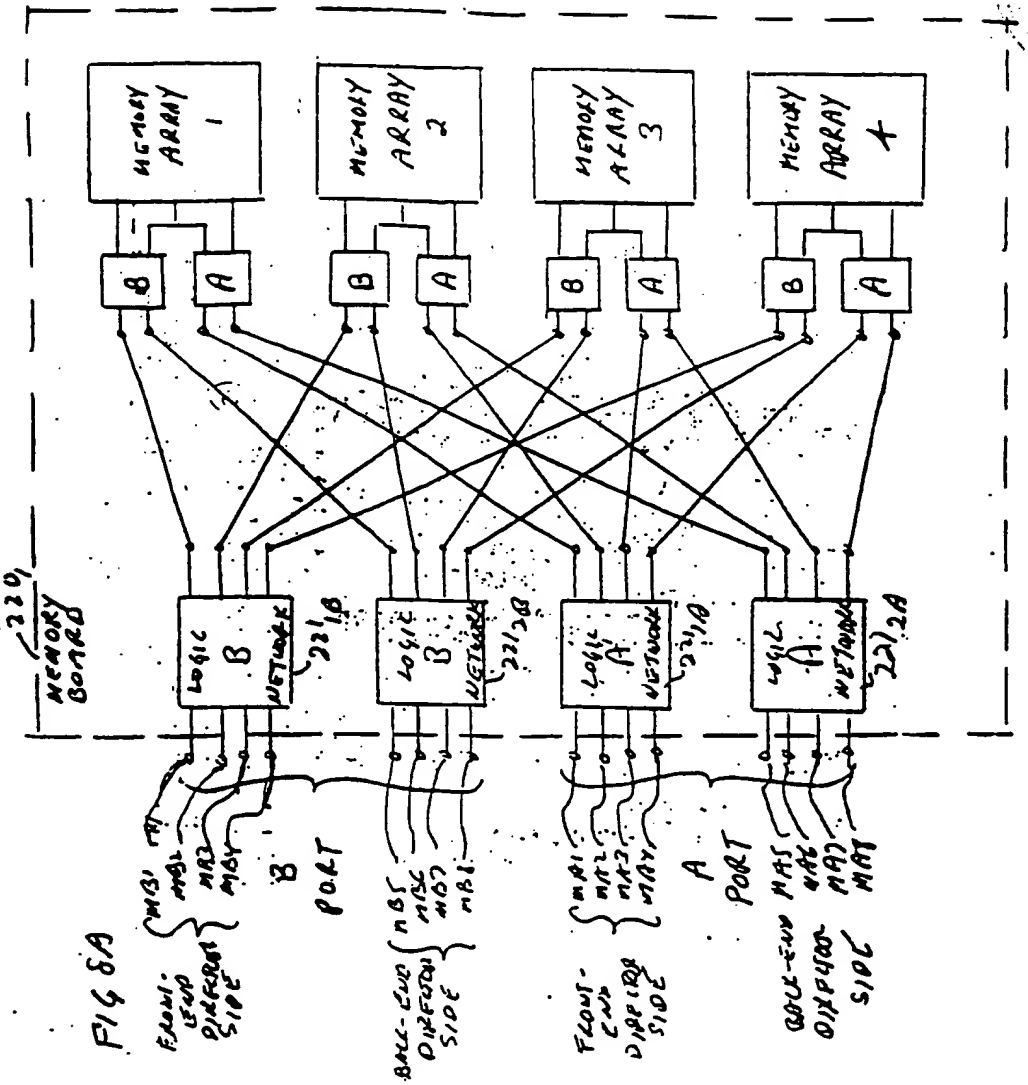

MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4
B
A
220
MEMORY BOARD
LOGIC
NETWORK
221/1B
221/2B
221/1A
221/2A
B PORT
A PORT

FIG 8A

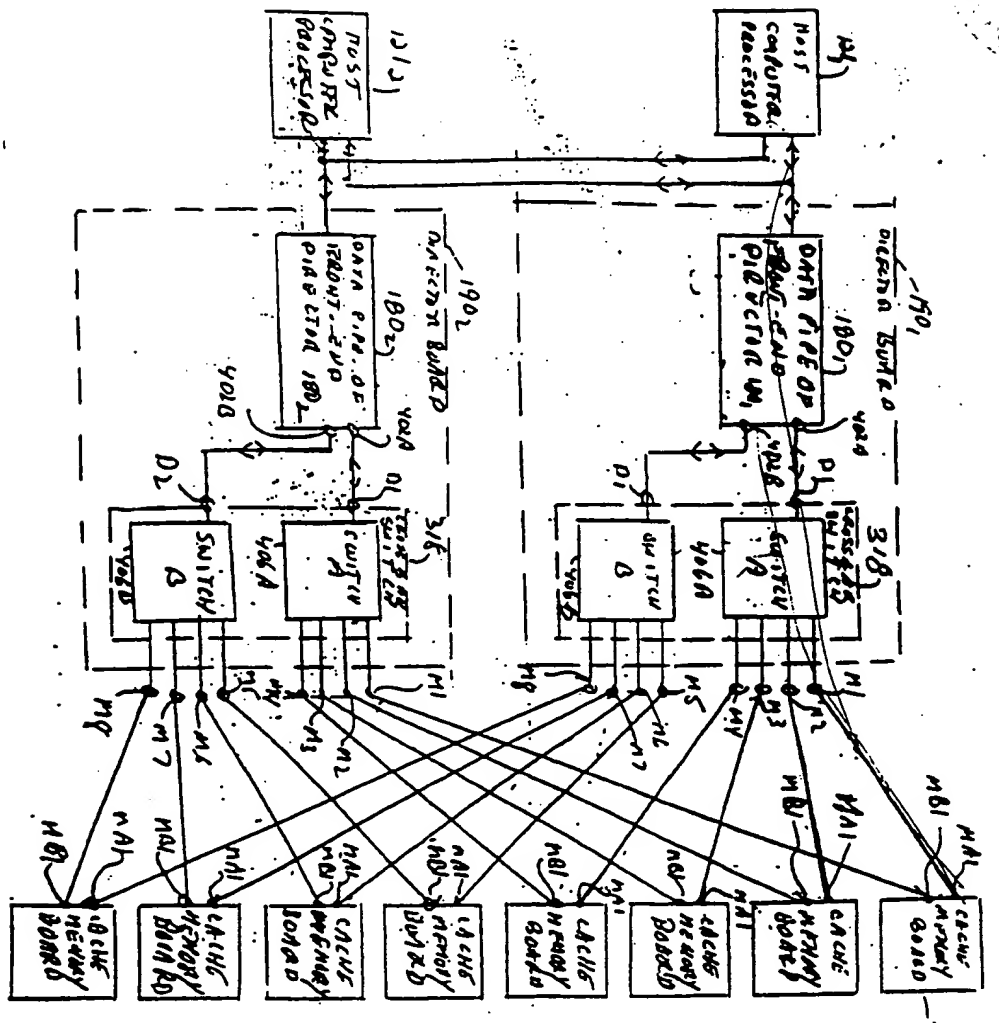


FIG 8B

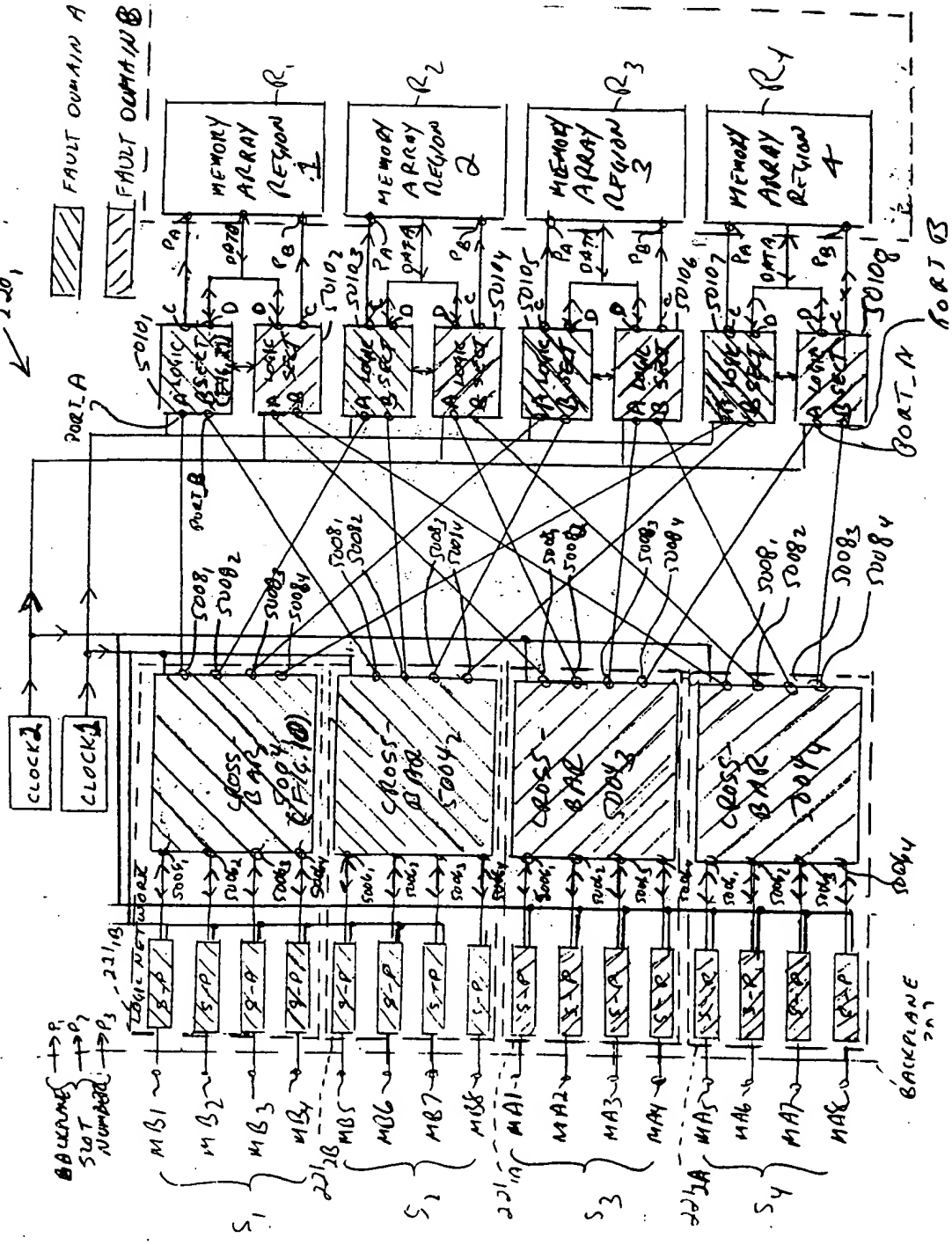

FAULT DOMAIN A
FAULT DOMAIN B
MEMORY ARRAY REGION 1
MEMORY ARRAY REGION 2
MEMORY ARRAY REGION 3
MEMORY ARRAY REGION 4
PORT_A
PORT_B
CLOCK2
CLOCK1
CROSS BAR SW4
BACKPLANE

FIG. 9

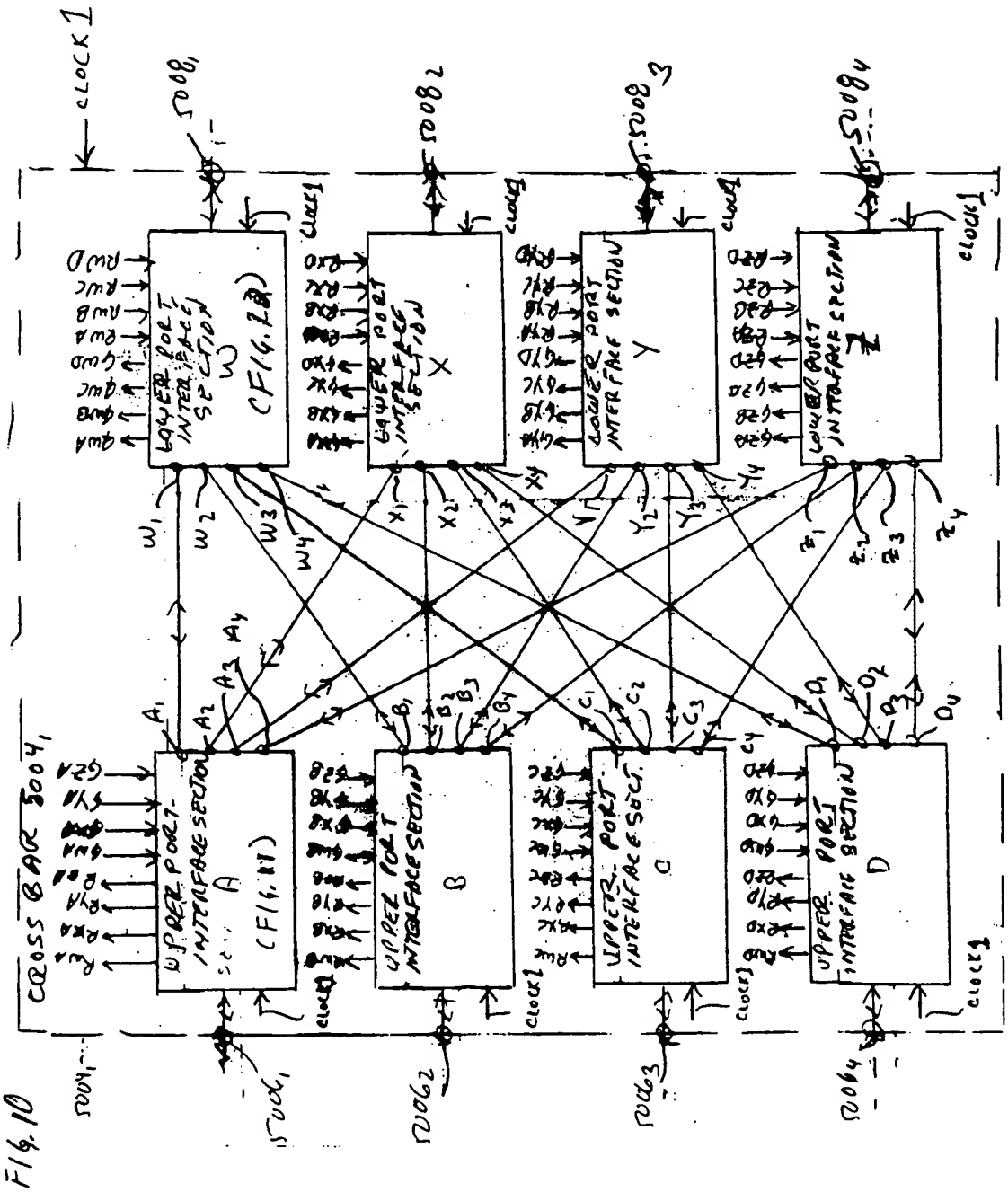

CROSS BAR 300
CLOCK 1
UPPER PORT INTERFACE SECTION A
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECT. C
UPPER PORT INTERFACE SECTION D
LOWER PORT INTERFACE SECTION W
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
CLOCK 1

FIG. 10

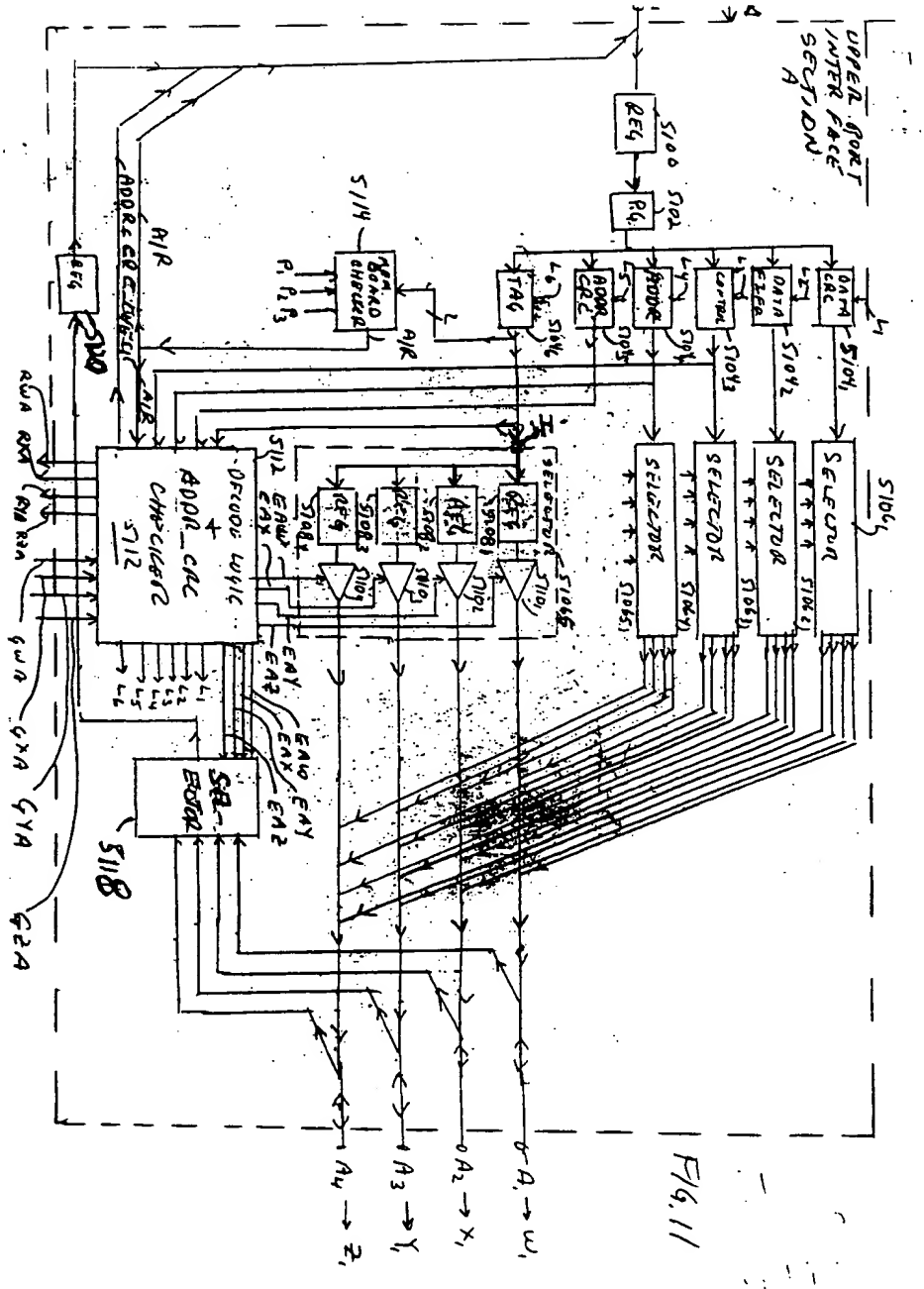

UPPER PORT INTER FACE SECTION
REG
5100
5102
5114
BOARD ADDRESS
P1 P2 P3
ADDR
ADDR CRC
TAG
CONTROL
DATA FIELD
DATA CRC
5104
5106
5108
5110
5112
ADDR CRC CHECKER
5118
SELECTOR
A1 → W1
A2 → X1
A3 → Y1
A4 → Z1

FIG. 11

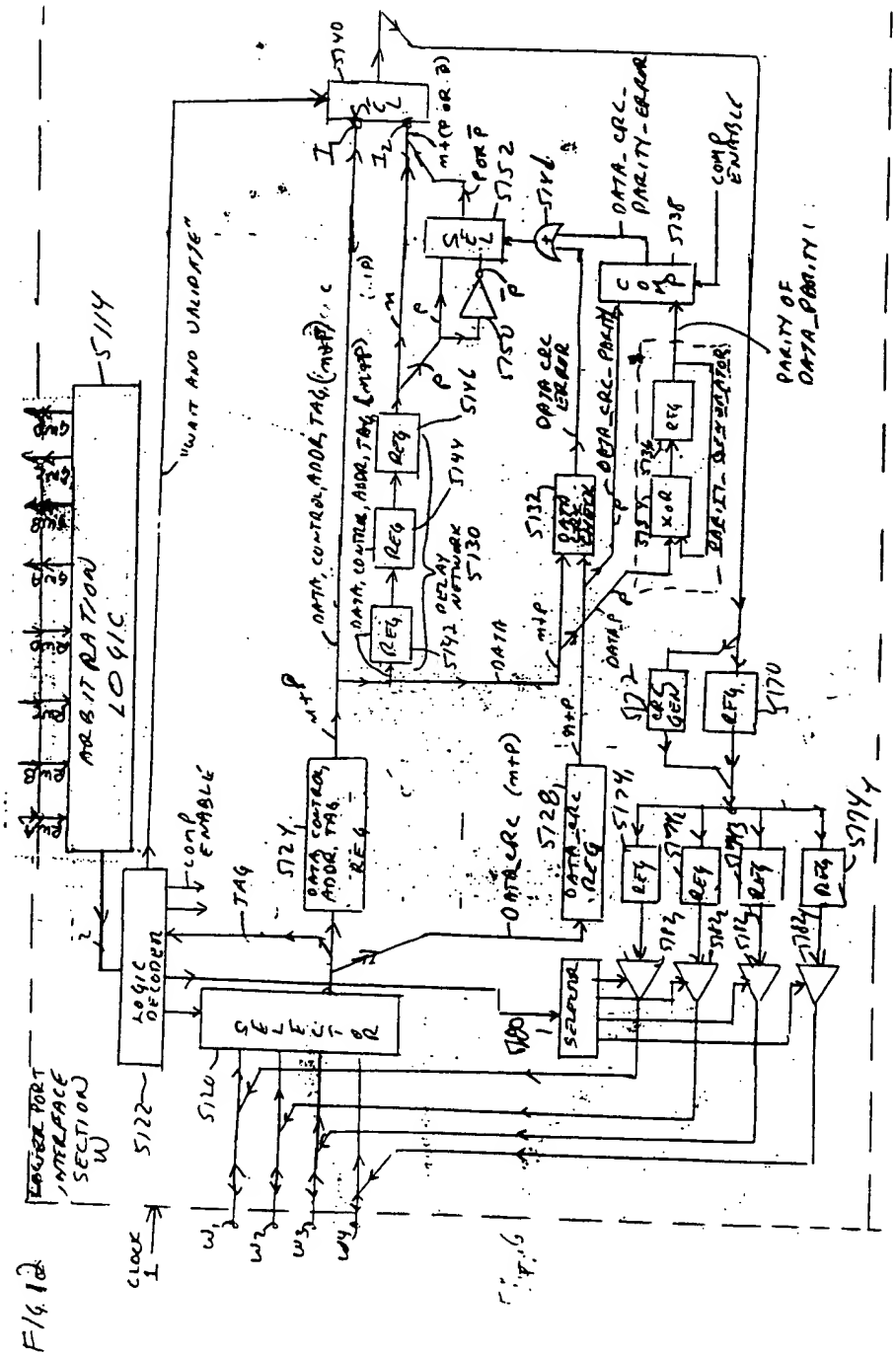
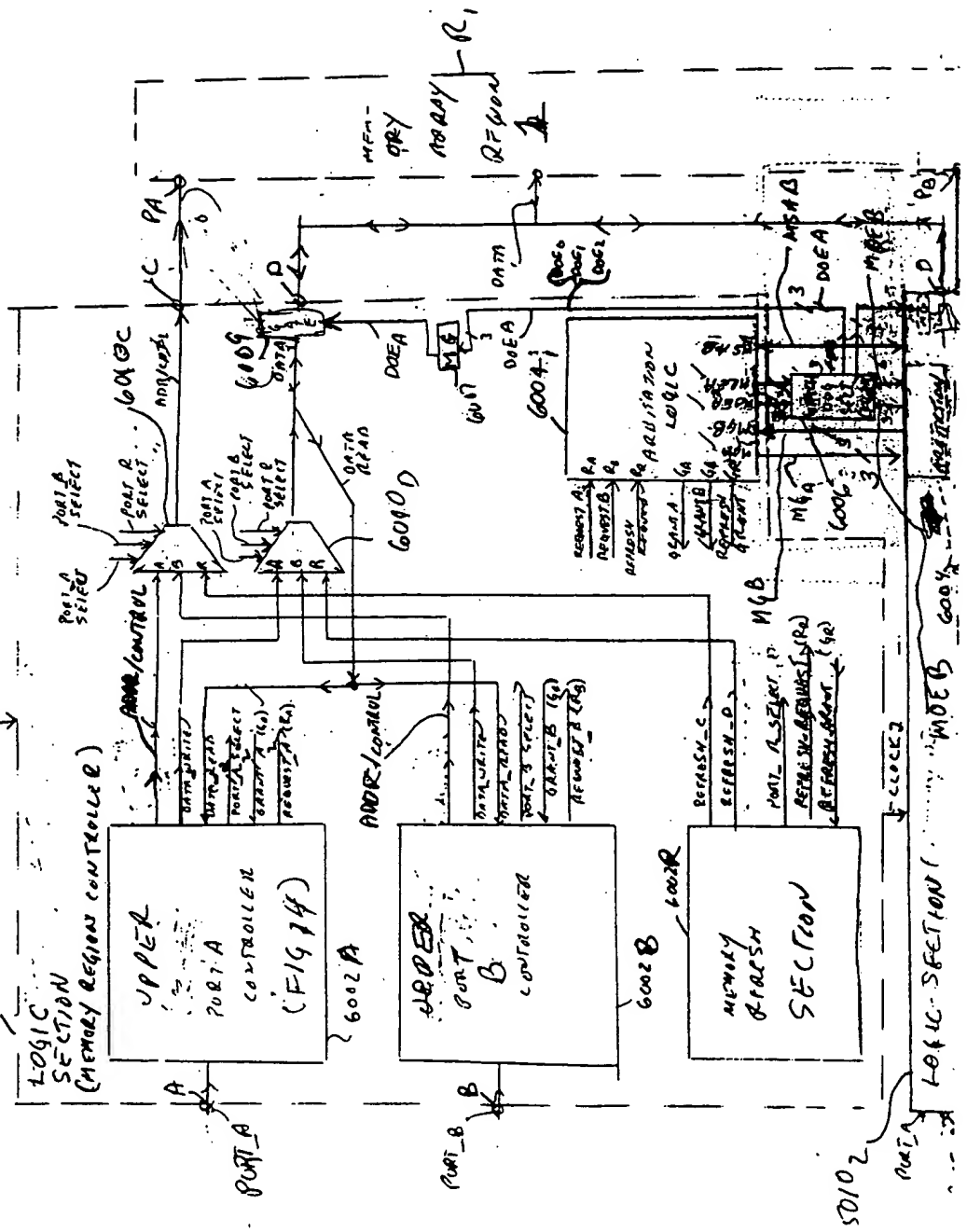

ARBITRATION LOGIC
"WAIT AND UNLOCK"
LOGIC DECODER
SELECTOR
DATA, CONTROL, ADDR, TAG, (m+p)
DATA
DATA CRC ERROR
DATA_CRC_PARITY
PARITY OF DATA_PARITY
COMP ENABLE
TAG
CLOCK
DELAY NETWORK
REG
XOR
COMP
GEN

Fig. 1a


LOGIC SECTION (MEMORY REGION CONTROLLER)
5010
CLOCK1
UPPER PORT A CONTROLLER (FIG 1F)
6002A
UPPER PORT B CONTROLLER
6002B
MEMORY REFRESH SECTION
6002C
6004
6006
6008
6009
MEMORY ARRAY
ADDR/CONTROL
DATA READ
PORT A SELECT
PORT B SELECT
REFRESH_C
CLOCK2
PORT_A
PORT_B
5010
LOGIC SECTION

F/G. 1B

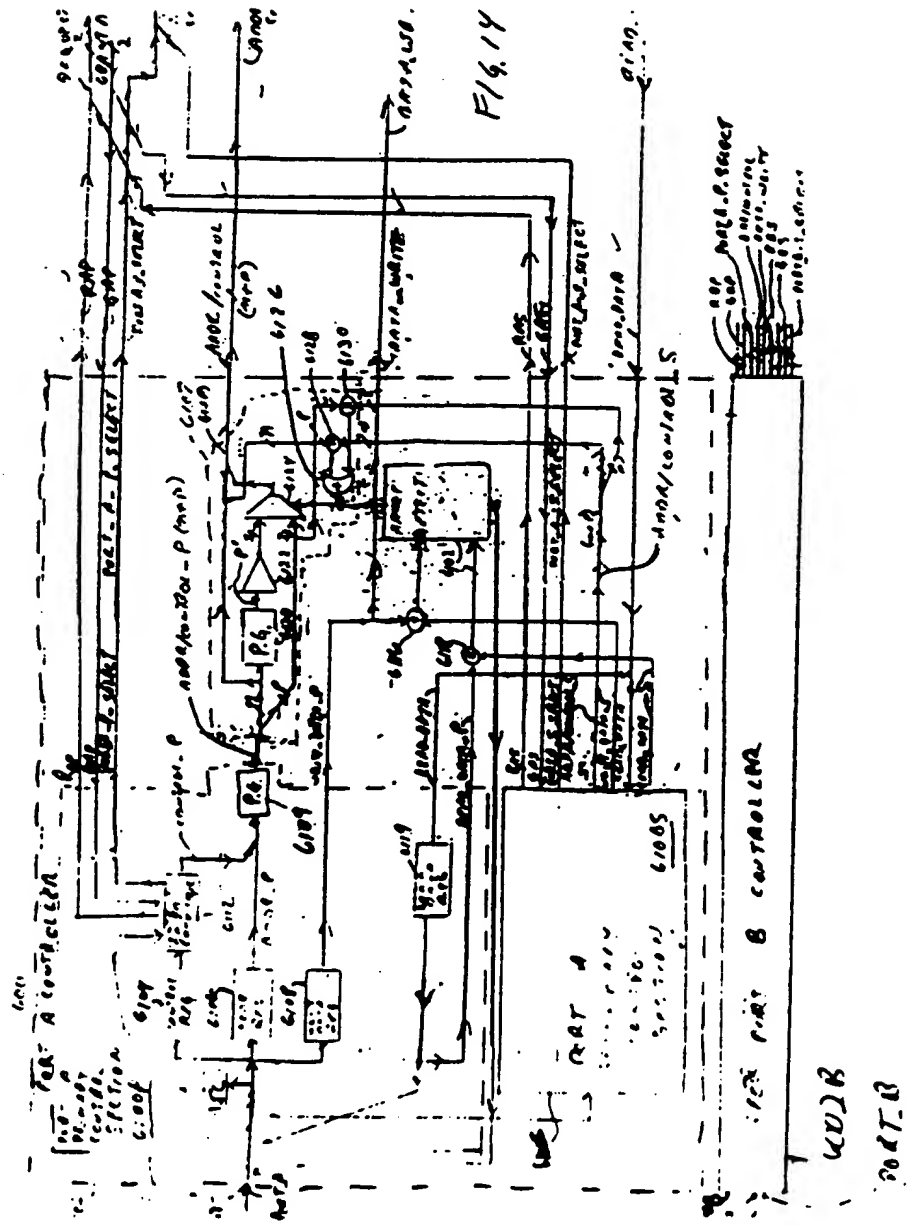
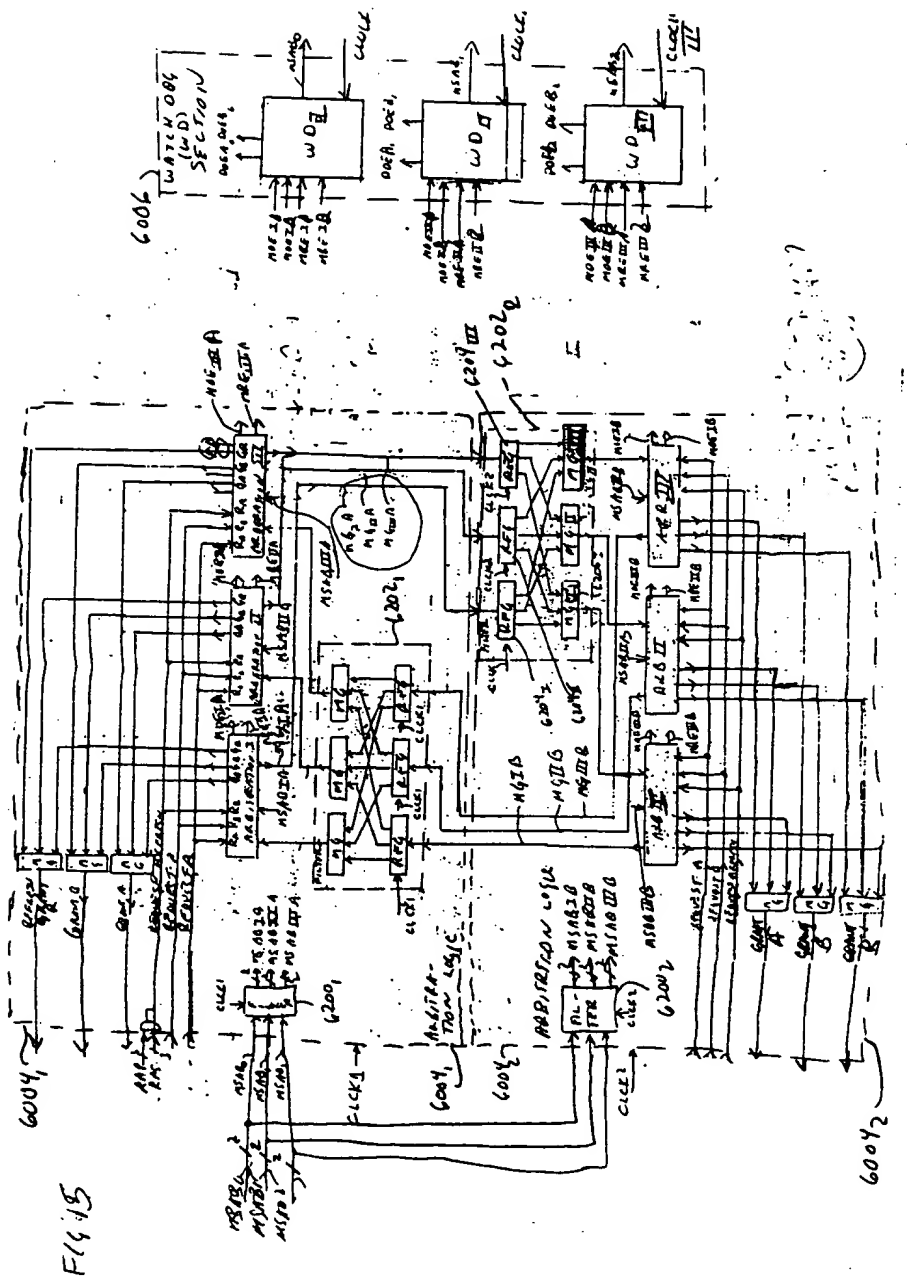


FIG. 14



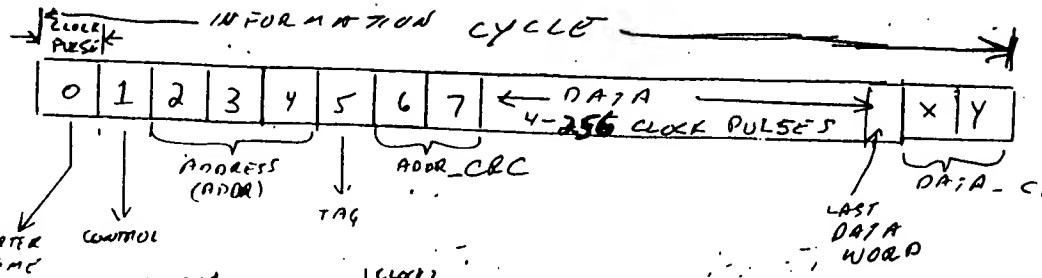


FIG. 16

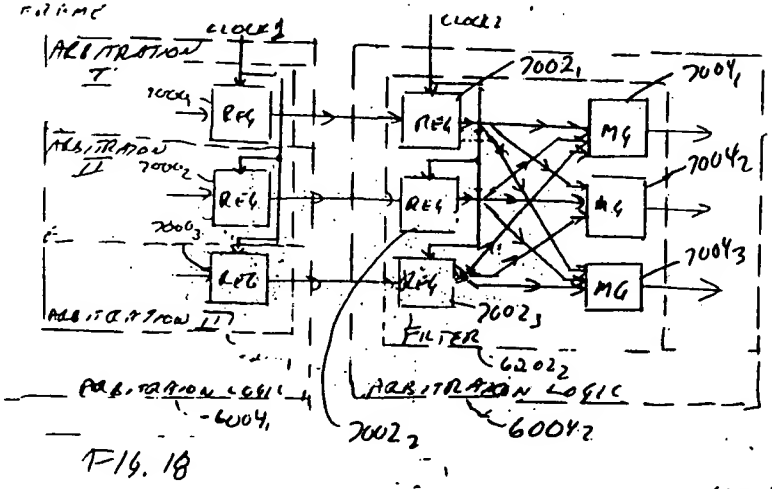


FIG. 18

FIG. 17

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	1	1	1
1 0 0	0	0	0
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	1	1	1

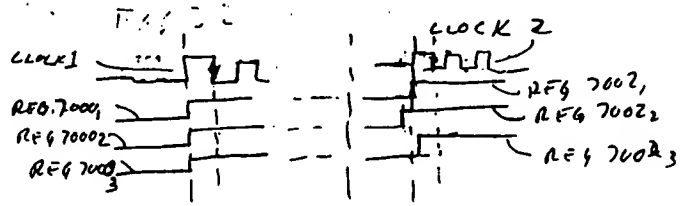
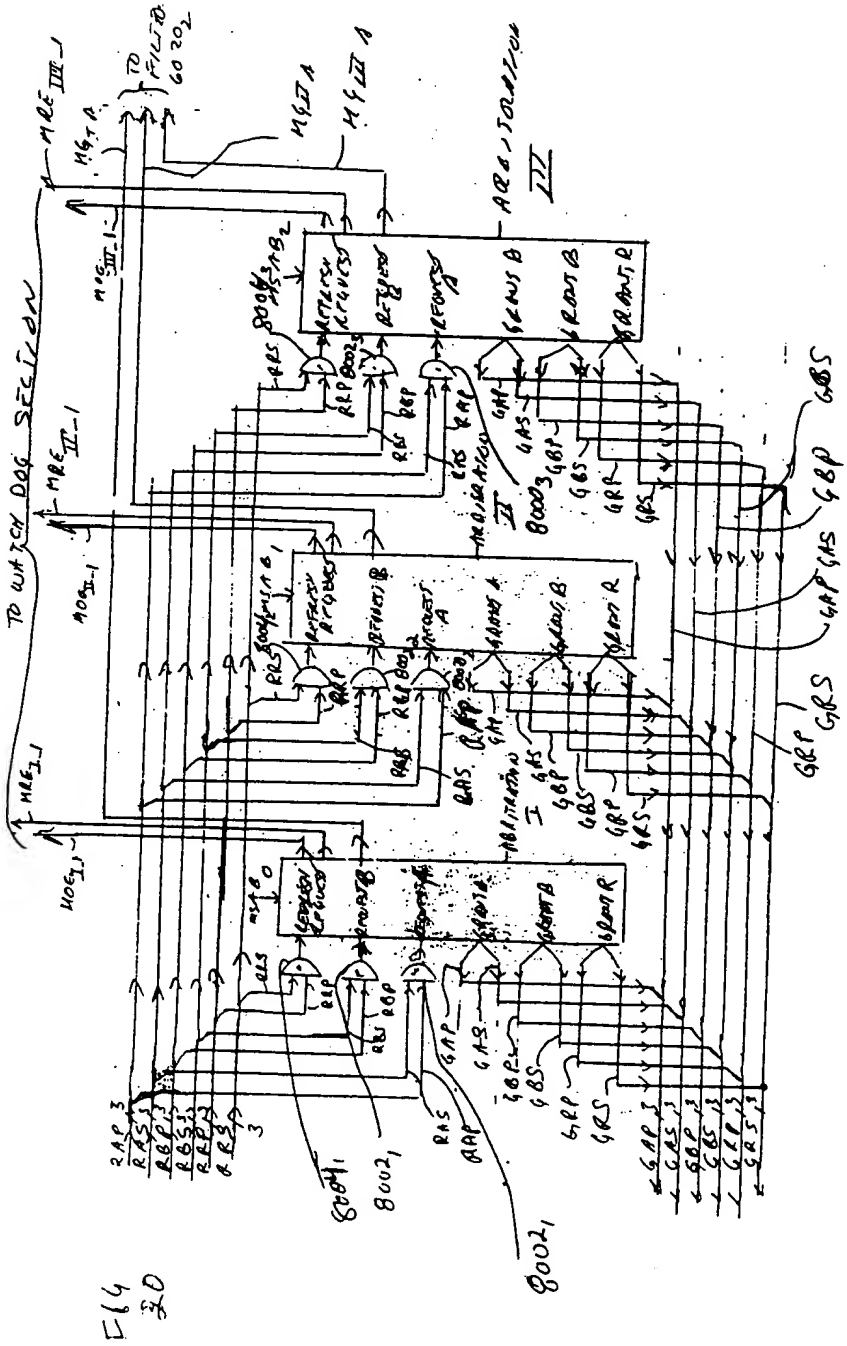



FIG. 19